REMARKS

By the present amendment, claims 1 and 14 have been amended. Thus, after the present amendment, claims 1, 3-15, 17-23, and 25 remain in the present application. Reconsideration and allowance of outstanding claims 1, 3-15, 17-23, and 25 in view of the above amendments and following remarks are requested.

A. Rejections of Claims 1, 3-15, 17-23, and 25 under 35 USC §103(a)

The Examiner has rejected claims 1, 3-15, 17-23, and 25 under 35 USC §103(a) as being unpatentable over U.S. Patent Number 5,436,177 to Zaccherini ("Zaccherini"), U.S. Patent Number 5,489,547 to Erdeljac et al., and U.S. Patent Number 6,156,602 to Shao et al. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 14, is patentably distinguishable over Zaccherini, Erdeljac, and Shao.

As disclosed in the present application, at pages 14 and 15 and Figure 2, a silicide blocking oxide layer (e.g. silicon oxide layer 206) is formed above the resistor material (i.e. above polycrystalline silicon layer 202). The electrical conductivity of the contact regions is then enhanced by P+ doping the exposed regions of polycrystalline layer 202 not covered by silicon oxide layer 206. Contact regions are then formed on the polycrystalline layer comprising the high resistivity resistor. Consequently, embodiments according to the present invention advantageously achieve a high resistivity resistor having a low fabrication cost and improved electrical connectivity.

Amended independent claims 1 and 14 further recite "forming a silicide blocking oxide layer over an inner portion of said layer over said field oxide region; doping an outer portion of said layer over said field oxide region with a third dopant so as to form a high-doped region in said outer portion of said layer over said field oxide region, wherein said third dopant has said second conductivity type." Amended independent claims 1 and 14 further include language indicating that that the transistor gate region is situated over a well and field oxide region 208 is not situated over the well.

In contrast to the present invention as defined by amended independent claims 1 and 14, Zaccherini is directed to a process for forming implanted regions with a lowered channeling risk on semiconductors. The semiconductor devices include at least one layer of polycrystalline silicon that covers all isolation regions and active areas that are liable to a channeling phenomenon.

Zaccherini discloses forming P-doped resistors in predetermined area 8 of polycrystalline layer 7 overlying field oxide 5, which is situated on doped epitaxial layer 3. See, for example, column 3, lines 15-23 and Figure 4 of Zaccherini. In Zaccherini, transistor 1 is formed on doped epitaxial layer 3, which covers substrate 2. See, for example, column 2, lines 54-55 and Figure 4 of Zaccherini. Thus, in Zaccherini, predetermined area 8 and transistor 1 are both situated on epitaxial layer 3. However, Zaccherini fails to disclose, teach, or even suggest a transistor gate region situated over a well and a field oxide region, over which a high resistivity resistor is formed, not being situated over the well. Furthermore, the Examiner even states, correctly, that Zaccherini

fails to teach that the transistor gate region is situated over a well and field oxide region 208 is not situated over the well.

Additionally, Zaccherini does not even suggest "forming a silicide blocking oxide layer over an inner portion of said layer over said field oxide region; doping an outer portion of said layer over said field oxide region with a third dopant so as to form a high-doped region in said outer portion of said layer over said field oxide region, wherein said third dopant has said second conductivity type," as recited in amended independent claims 1 and 14. Zaccherini provides no motivation for forming a high-doped region in the layer over the field oxide region or even mention any method of completing formation of resistors in predetermined area 8 of polycrystalline layer 7.

Zaccherini does not disclose, teach, or suggest the configuration of amended independent claims 1 and 14. Furthermore, there is no teaching or suggestion to combine or modify Zaccherini. Therefore, Zaccherini, singly or in combination with other art of record, does not disclose, teach, or suggest the present invention as defined by amended independent claims 1 and 14.

Erdeljac does not cure the deficiencies of Zaccherini. Erdeljac is directed to a semiconductor device having p-type polysilicon resistor 56 with a moderate sheet resistance and low temperature of coefficient resistance. A double-level polysilicon process is implemented. This process additionally is used to create n- and p-channel transistors, a capacitor, an n-type polysilicon resistor having a high sheet resistance, and an n-type resistor having a low resistance.

The Examiner argues that Erdeljac teaches a transistor gate region being situated over a well and a field oxide region not being situated over the well. However, there is no teaching or suggestion to combine the teachings of Erdeljac with the process disclosed in Zaccherini. Furthermore, Zaccherini does not teach the advantages of implementing the process of the claimed configuration.

Moreover, the Examiner states, correctly, that the combined teachings of Zaccherini and Erdeljac fail to teach "doping a portion of said transistor region of said polycrystalline silicon layer with a third dopant so as to form a high-doped region in said transistor region, wherein said third dopant has said second conductivity type; and fabricating a contact region over said high-doped region in said resistor region of said polycrystalline silicon layer, wherein said contact region being electrically connected to said resistor region."

Upon a further comparison of the teachings of Erdeljac to the present invention as defined by amended independent claims 1 and 14, it is apparent that Erdeljac does not teach "forming a silicide blocking oxide layer over an inner portion of said layer over said field oxide region; doping an outer portion of said layer over said field oxide region with a third dopant so as to form a high-doped region in said outer portion of said layer over said field oxide region, wherein said third dopant has said second conductivity type," or the advantages thereof.

Thus, Erdeljac does not disclose, teach, or suggest the configuration of amended independent claims 1 and 14. Furthermore, there is no teaching or suggestion to combine

or modify Erdeljac. Therefore, Erdeljac, singly or in combination with other art of record, does not disclose, teach, or suggest the present invention as defined by amended independent claims 1 and 14.

Shao does not cure the deficiencies of Zaccherini and Erdeljac. Shao is directed to a method for forming a poly resistor of accurate value that is required in mixed-mode configurations (i.e. applications where capacitors coexist with logic applications on the same integrated circuit.) More specifically, Shao discloses performing N+ implant 18 into poly 2 layer 16 to form the conductivity level of an NMOS poly gate and also to control the value of a load resistor, i.e. load resistor 38, which is also formed in poly 2 layer 16 over field oxide region 12. See, for example, column 5, lines 7-26 and Figures 1 and 5 of Shao. In Shao, NMOS gate 40 and load resistor 38 are both situated over substrate 10. See, for example, Figure 5 of Shao. However, Shao fails to teach, disclose, or suggest a transistor gate region situated over a well and a field oxide region, over which a high resistivity resistor is formed, not being situated over the well.

In Shao, after load resistor 38 has been formed, an N+ implant of contact regions 72 and 74 of load resistor 38 is performed. See, for example, column 7, lines 64-65 and Figure 6 of Shao. However, Shao does not teach "doping a portion of said transistor region of said polycrystalline silicon layer with a third dopant so as to form a high-doped region in said transistor region, wherein said third dopant has said second conductivity type; and fabricating a contact region over said high-doped region in said resistor region

of said polycrystalline silicon layer, wherein said contact region being electrically connected to said resistor region."

For example, Shao does not teach, disclose, or suggest doping poly 2 layer 16 with a second dopant so as to form a high resistivity resistor in poly 2 layer 16 over field oxide region 12. Further, in Shao, a doping barrier above the layer over field oxide region 12, i.e. the resistor region, is not even implemented.

Shao does not disclose, teach, or suggest the configuration of amended independent claims 1 and 14. Furthermore, there is no teaching or suggestion to combine or modify Shao. Therefore, Shao, singly or in combination with other art of record, does not disclose, teach, or suggest the present invention as defined by amended independent claims 1 and 14.

For the foregoing reasons, Applicants respectfully submit that the present invention as defined by amended independent claims 1 and 14 is not taught, disclosed, or suggested by the art of record. Thus, amended independent claims 1 and 14 are patentably distinguishable over the art of record. As such, the claims depending from amended independent claims 1 and 14 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1 and 14, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 1, 3-15, 17-23, and 25 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to all claims 1, 3-15, 17-23, and 25 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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